[0020.2] Another embodiment of the present invention is a virtual ground-type memory integrated circuit comprising a plurality of word select lines; a plurality of column lines; a memory array having a plurality of adjustable threshold voltage memory transistors, each being programmable using channel hot electron injection and having a source coupled to one of the column lines, a drain coupled to an adjacent one of the column lines, a floating gate overlying a channel defined in a substrate body region between the source and the drain, and a control gate overlying the floating gate and coupled to one of the word select lines; a voltage source for applying a body voltage to the substrate body regions containing the channels; a voltage source for applying a reference voltage to the sources of at least a first and a second of the memory transistors via a first one of the column lines; a voltage source for applying a programming voltage to the drains of the first and second memory transistors via a second one of the column lines adjacent the first column line, the reference and programming voltages being sufficient to generate channel hot electrons in the respective channels of the first and second memory transistors; a voltage source for applying a select voltage to the gate of the first memory transistor via a first one of the word select lines, the select voltage having a polarity and magnitude relative to the body voltage sufficient to attract the hot electrons of the first memory transistor and change the threshold voltage thereof to a programmed state; and a voltage source for applying an unselect voltage to the gate of the second memory cell via a second one of the word select lines, the unselect voltage having a polarity and magnitude relative to the first voltage sufficient to repel the hot electrons of the second memory transistor and deter change in the threshold voltage thereof.

Kindly delete paragraph [0021].

Kindly delete paragraph [0022].

[REST OF PAGE INTENTIONALLY BLANK]

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